REMARKS

Claims 1-16 are pending in this application. Claims 1-14 stand rejected. By this Amendment, claim 1 has been amended and new claims 15 and 16 have been added. No new matter has been added. The amendments made to the claims do not alter the scope of these claims, nor have these amendments been made to define over the prior art. Rather, the amendments have been made to improve the form thereof. In light of the amendments and remarks set forth below, Applicants respectfully submit that each of the pending claims is in immediate condition for allowance.

Applicants note that the Information Disclosure Statement submitted July 22, 2005 by Applicant has not been initialed by the Examiner and returned. Applicants include herewith a copy of the PTO SB08 and request that the Examiner initial and return the same to Applicants.

Claims 1, 2, and 4-8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,026,485 ("O'Connor"). Applicants respectfully request reconsideration and withdrawal of this rejection.

Among the limitations of independent claim 1 not present in the cited reference is a registered memory configuration unit designed to configure the register memory such that the memory space in the register memory is assigned to operands and that memory space in the register memory that is not assigned to operands is made available for data other than the operands.

The Office Action equates the register memory configuration unit with the stack management unit disclosed in O'Connor. However, the stack management unit in O'Connor does not perform the explicitly recited function of Applicants' register memory configuration unit.

O'Connor, stack management unit 150 supports both stack 400b and execution environment memory 440. Specifically, stack management unit 150 adds an execution environment stack cache 450, an execution environment dribble manager unit 460, and an execution environment stack control unit 470. The dribble manager unit transfers an entire execution environment between execution environment 450 and execution environment memory 440 during a spill operation or a fill operation. The stack management unit 150 stores information and provides operands to execution unit 140. Stack management unit 150 also takes care of overflow and underflow conditions of the stack cache 155. The stack cache 155 is managed in a circular buffer which ensures that the stack grows and shrinks in a predictable manner to avoid overflows or overwrites. The saving and restoring of values to and from data cache 165 is controlled by a dribble manager. As such, stack management unit 150 merely places the above data in randomly accessible storage 810. However, it is noted that randomly accessible storage 810 has constant area 814 for implementing the Java virtual machine for commonly used constants. As such, while the stack management unit is used to fill the memory 810, there are predefined constant locations and thus, O'Connor fails to disclose the memory configuration unit designed to configure the register memory such that the memory space in the register memory that is not assigned to operands is made available for data other than the operands. Therefore, Applicants respectfully submit that claim 1 is allowable over O'Connor.

Claims 2-8 depend from, and contain all the limitations of claim 1. These dependent claims also recite additional limitations which, in combination with the limitations of claim 1, are neither disclosed nor suggested by O'Connor and are also believed to be directed towards the patentable subject matter. Thus, claims 2-8 should also be allowed.

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over O'Connor in view of U.S. Patent No. 6,185,596 ("Hadad"). Hadad was not added to cure the deficiency in O'Connor noted above but to show additional limitations which, even if they were to show, do not cure the deficiencies discussed above. As such, Applicants respectfully submit that the claims are allowable over the cited references.

Therefore, Applicants respectfully submit that claim 3 is allowable over the cited combination.

Claims 9-11 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,777,589 ("Boettner"). Applicants respectfully request reconsideration and withdrawal of this rejection.

Among the limitations of independent 9 not present in the cited reference is a memory configuration unit, the memory configuration unit being designed to make space from the internal memory available for the peripheral device, as needed.

In Boettner, virtual memory systems are accessed by one of two methods. In the first method, special instructions are provided within the computer instruction set which control IR devices. In the second method, referred to as memory map I/O, certain addresses are reserved for each I/O device. However, at no time does Boettner disclose that the memory is configurable as needed. Therefore, Applicants respectfully submit that claim 9 is allowable over Boettner.

Claims 10-14 depend from, and contain all the limitations of claim 9. These dependent claims also recite additional limitations which, in combination with the limitations of claim 9, are neither disclosed nor suggested by Boettner and are also believed to be directed towards the patentable subject matter. Thus, claims 10-14 should also be allowed.

Applicants include two additional independent claims, claims 15 and 16. The claims include a volatile working memory, an external working memory, and the register memory which is not part of the external working memory. Furthermore, at least a part of the register memory is mapped into the working memory, so that an address unit is operable to address the memory space not assigned to operands by the register memory configuration unit in the same way as the external working memory.

Thus, the present claims provide optimum memory usage ensuring that the available memory space is available for improving the performance of the processor, even though the register memory is not used by operands of the arithmetic unit for a certain task. In environments in which the chip area for memory is limited such as in the field of chip cards, the present invention is particularly useful, since the chip designer can assign a large-enough register memory without having to fear that the large register area constitutes a waste of chip area for cases, in which the arithmetic unit does not have to process such large operands. Further advantages are described in the specification at least at pages 4, 5, 8.

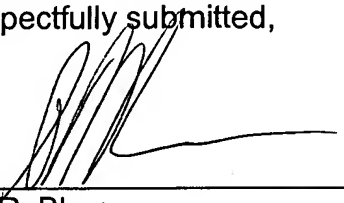
Applicants have responded to all of the rejections and objections recited in the Office Action. Reconsideration and a Notice of Allowance for all of the pending claims are therefore respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

If the Examiner believes an interview would be of assistance, the Examiner is welcome to contact the undersigned at the number listed below.

Dated: September 28, 2006

Respectfully submitted,



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